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Application No.: 10/823,489 Docket No.: JCLA12709

Amendments

In The Claims:

Please amend the claims as follows:

1. (currently amended) A power supply with multiple outputs, comprising:

a front-end converter with a current mode output;

a first buck converter and a second buck converter, both of which cascade from a first output capacitor of the front-end converter; and

a time delay synchronous control circuit, for controlling a delay time between the time the front-end converter begins to have a pulse current to the first output capacitor and the time the first buck converter and the second buck converter being turned on is adjusted, wherein

the first buck converter and the second buck converter draw pulse current from the first output capacitor during the time when the front-end converter has the pulse output current to the first output capacitor.

2. (original) The power supply with multiple outputs of claim 1, wherein the front-end converter is a LLC-SRC.

3. (original) The power supply with multiple outputs of claim 1, wherein the front-end converter comprising:

a bridge circuit including a pair of power switches, the bridge circuit being coupled to an input voltage;

a resonant tank, coupled to the bridge circuit, being driven by the pair of power switches; and

a rectifier, coupled to the resonant tank, for providing the current mode output of the front-end converter from the resonant tank.

4. (original) The power supply with multiple outputs of claim 3, wherein the rectifier is a diode rectifier or a synchronous rectifier.

5. (original) The power supply with multiple outputs of claim 3, wherein the resonant tank comprising:

a series resonant capacitor, coupled to the bridge circuit;

a series resonant inductor, coupled to the series resonant capacitor; and

a transformer with a magnetizing inductor coupled to the series resonant inductor and the bridge circuit,

wherein the series resonant capacitor, the series resonant inductor and the magnetizing inductor constitute two characteristic frequencies of the resonant tank.

6. (original) The power supply with multiple outputs of claim 5, wherein the series resonant inductor is a discrete component for the transformer or is replaced by the leakage inductance of the transformer.

7. (original) The power supply with multiple outputs of claim 3, wherein the bridge circuit comprises a bus capacitor coupled to the input voltage.

8. (original) The power supply with multiple outputs of claim 5, wherein the transformer comprising a primary winding and two secondary windings connected in series in phase, for isolating the bridge circuit and the resonant tank from the rectifier.

9. (original) The power supply with multiple outputs of claim 3, wherein the rectifier is a full-wave rectifier comprising a first rectifier diode and a second rectifier diode connected to the output capacitor, the first and second rectifier diodes are connected through the output capacitor to an output filter to generate an output voltage of the multiple outputs of the power supply.

10. (original) The power supply with multiple outputs of claim 9, wherein an anode of the first rectifier diode is connected to a nominal terminal of a first secondary winding of the transformer and an anode of the second rectifier diode is connected to a reverse terminal of a second secondary winding of the transformer, a connection terminal of the first and second secondary windings is connected to the output as the ground of a secondary side of the transformer.

11. (original) The power supply with multiple outputs of claim 1, wherein after the delay time behind the time when the front-end converter begins to have the pulse output current, the first buck converter and the second buck converter are sequentially turned on and then the first

buck converter is turned off after the second buck converter is turned off.

12. (original) The power supply with multiple outputs of claim 1, wherein buck switches of both the first and second buck converters are turned off before the pulse output current of the front-end converter reaches to zero.

13. (original) The power supply with multiple outputs of claim 1, wherein after the delay time behind the time when the front-end converter begins to have the pulse output current, the first buck converter is turned on and then the first buck converter is turned off, at the time the first buck converter being turned off, the second buck converter is sequentially turned on.

14. (original) The power supply with multiple outputs of claim 1, wherein a dead conduction time interval exists between every two of the output current pulses of the front-end converter, the first buck converter and the second buck converter are sequentially turned on and then the first buck converter is turned off before the second buck converter is turned off, an overlap existing between the period of the first buck converter being on and the period of the second buck converter being on.

15. (original) A power supply with multiple outputs, comprising:

a front-end converter with a current mode output, for providing a first output of the power supply; and

a first buck converter and a second buck converter, both of which cascade a first output

capacitor of the front-end converter and the outputs of which are connected together for providing a second output of the power supply; and

a time delay synchronous control circuit, for controlling the first buck converter and the second buck converter alternatively drawing one of the two pulse currents from the first output capacitor during the time when every two pulse of the output current of the front-end converter are provided, and during the time of each pulse of the output current of the front-end converter, only one of the first buck converter and the second buck converter drawing the pulse current from the first output capacitor.

16. (original) The power supply with multiple outputs of claim 15, wherein a delay time exists between the time the front-end converter begins to have the pulse output current and the time the first buck converter or the second buck converter are turned on.

17. (original) The power supply with multiple outputs of claim 15, wherein both of the first and second buck converters are turned off before the pulse output current of the front-end converter reaches to zero.

18. (original) A time delay synchronous control method for a power supply with multiple outputs, the power supply comprising a front-end converter with a current mode output and a first buck converter and a second buck converter, both of which cascade an output capacitor of the front-end converter, the first buck converter being controlled by a first buck switch and the second buck converter being controlled by a second buck switch, the method comprising:

adjusting a delay time between the time the front-end converter begins to have the pulse output current to the output capacitor and the time the first buck switch and the second buck switch being turned on; and

drawing pulse output current from the first output capacitor by the first buck switch and the second buck switch during the time when the front-end converter has the pulse output current to the first output capacitor.

19. (original) The time delay synchronous control method of claim 18, wherein after the delay time behind the time when the front-end converter begins to have the pulse output current, the first buck switch and the second buck switch are sequentially turned on and then the first buck switch is turned off after the second buck switch being turned off.

20. (original) The time delay synchronous control method of claim 19, wherein after the delay time behind the time when the front-end converter begins to have the pulse output current, the first buck switch is turned on and then the first buck switch is turned off, at the time the first buck switch being turned off, the second buck switch being sequentially turned on.

21. (original) The time delay synchronous control method of claim 18, wherein a dead conduction time interval exists between every two of the output current pulses of the front-end converter, the first buck switch and the second buck switch being sequentially turned on and then the first buck switch is turned off before the second buck switch being turned off, a overlap existing between the period of the first buck switch being on and the period of the second buck

switch being on.

22. (currently amended) A power supply with multiple outputs, comprising :

a converter with a main switch, a rectifier and a output capacitor; and

a buck converter, directly cascading the output capacitor of the converter, wherein the buck converter is controlled by a buck switch, the buck switch begins to turn on ~~synchronously with the rectifier at the time the converter turns off~~ at the time when the converter has a pulse current to the output capacitor and turn off at the time before the time when the ~~converter~~ main switch turns on.

23. (original) The time delay synchronous control scheme of claim 22, wherein the converter is a flyback converter.

24. (original) The time delay synchronous control scheme of claim 22, wherein the rectifier is a diode rectifier or a synchronous rectifier.